FUEL YOUR INSIGHT
LLVM Framework and IR Extensions for Parallelization, SIMD Vectorization and Offloading

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Agenda

- Motivation
- Design Principles
- Pros / Cons Analysis for LLVM IR Extension Options
- LLVM IR Extensions and W-Region Framework
- Parallelization and Vectorization Framework,
- Code Generation Examples
- Summary and Future Work
Motivating Example

Two adjacent OpenMP parallel for loops

```c
#pragma omp parallel for simd
for (i=0; i<N; ++i) { X[i] += sin(X[i]); }

#pragma omp parallel for simd
for (i=0; i<N; ++i) { Y[i] += cos(X[i]); }
```

With loop fusion, the granularity of the parallel for simd loop is increased, and the threading overhead is thus reduced

```c
#pragma omp parallel for simd
for (i=0; i<N; ++i) {
    X[i] += sin(X[i]);
    Y[i] += cos(X[i]);
}
```
Design Principles

- Add minimal extensions to the LLVM IR that are general enough to represent directives or pragmas.
- Minimize the impact on the existing LLVM infrastructure, and scalar/loop optimizations.
- Provide the framework support for directive (or pragma) based parallel, vector and offloading language extensions for modern CPUs, GPUs, coprocessors, DSP, and FPGA to explore target HW potential.
- Produce optimal threaded and/or vectorized code by leveraging existing and future scalar and loop optimizations with better interaction among optimization passes.
# Pros/Cons Analysis of LLVM IR Extensions Options

<table>
<thead>
<tr>
<th>Options</th>
<th>Pros</th>
<th>Cons</th>
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</thead>
<tbody>
<tr>
<td>A: add many new metadataes</td>
<td>No need to add new instructions or new intrinsics.</td>
<td>LLVM passes do not always maintain metadata. Must educate all passes to understand and handle them.</td>
</tr>
<tr>
<td>B: add a few new instructions</td>
<td>Parallelism becomes a first class citizen.</td>
<td>Huge effort for extending all LLVM passes and code generation to support new instructions. A large set of information still needs to be represented using other means.</td>
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<tr>
<td>C: add many new intrinsics</td>
<td>Less impact on the existing LLVM passes. No requirement for all passes to maintain metadata.</td>
<td>A large number of intrinsics to be added. Some of the optimizations need to be educated to understand them.</td>
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<tr>
<td>D: add a few intrinsics</td>
<td>Minimal impact on the existing LLVM optimizations passes. Only directive and clause names use metadata strings. No requirement for all passes to maintain metadata.</td>
<td>Some of the optimizations need to be educated to understand them.</td>
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LLVM Intrinsic Functions

// Directive and Qualifier Intrinsic Functions
def int_directive : Intrinsic<[],
    [llvm_metadata_ty], [IntrArgMemOnly], "llvmdirective">;
def int_directive_qual : Intrinsic<[],
    [llvm_metadata_ty],[IntrArgMemOnly],"llvmdirective.qual">;
def int_directive_qual_opnd : Intrinsic<[],
    [llvm_metadata_ty, llvm_any_ty],
    [IntrArgMemOnly], "llvm.directive.qual.opnd">;
def int_directive_qual_opndlist : Intrinsic<[],
    [llvm_metadata_ty, llvm_vararg_ty],
    [IntrArgMemOnly], "llvm.directive.qual.opndlist">;
# LLVM Intrinsics for Clauses

<table>
<thead>
<tr>
<th>No Operand</th>
<th>One Operand</th>
<th>List of Operands</th>
</tr>
</thead>
<tbody>
<tr>
<td>llvm.directive.qual</td>
<td>llvm.directive.qual.opnd</td>
<td>llvm.directive.qual.opndlist</td>
</tr>
<tr>
<td>✓ default</td>
<td>✓ num_threads</td>
<td>✓ shared</td>
</tr>
<tr>
<td>✓ nowait</td>
<td>✓ if</td>
<td>✓ private</td>
</tr>
<tr>
<td>✓ read</td>
<td>✓ final</td>
<td>✓ firstprivate</td>
</tr>
<tr>
<td>✓ write</td>
<td>✓ collapse</td>
<td>✓ lastprivate</td>
</tr>
<tr>
<td>✓ update</td>
<td>✓ ordered</td>
<td>✓ map</td>
</tr>
<tr>
<td>✓ capture</td>
<td>✓ simdlen</td>
<td>✓ depend</td>
</tr>
<tr>
<td>✓ untied</td>
<td>✓ safelen</td>
<td>✓ linear</td>
</tr>
<tr>
<td>✓ Mergeable</td>
<td>✓ priority</td>
<td>✓ uniform</td>
</tr>
<tr>
<td>✓ ... ...</td>
<td>✓ ... ...</td>
<td>✓ Reduction</td>
</tr>
<tr>
<td>✓ ... ...</td>
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<td>✓ ... ...</td>
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LLVM IR Example using Intrinsics

// C++ source code
#pragma omp parallel if(a) private(x, y, z)

// LLVM IR
%4 = load i32* @a, align 4
%5 = icmp ne i32 %4, 0
call void @llvmdirective(metadata !0)
call void @llvmdirective.qual.opnd(metadata !1, i32 %5)
call void @llvmdirective.qual.opndlist(metadata !3, %x, %y,
metadata !4, %z, %ctor, %dtor)
call void @llvmdirective(metadata !2)
... ... ...
!0 = metadata ![metadata !"DIR.OMP.PARALLEL"]
!1 = metadata ![metadata !"QUAL.OMP.IF"]
!2 = metadata ![metadata !"DIR.QUAL.LIST.END"]
!1 = metadata ![metadata !"QUAL.OMP.PRIVATE"]
!2 = metadata ![metadata !"QUAL.OPND.NONPOD"]
Privatization Semantics under SSA Form

- **private**: Alloca, Def, Use.
- **firstprivate**: Alloca, Copy-in, Def, Use
- **lastprivate**: Alloca, Def, Use, Copy-out
- **linear**: Alloca, Copy-in, Def, Use, Copy-out
- **reduction**: Alloca, Def, Use, Copy-in, Copy-out

✓ All “alloca instruction generated by the LLVM prepare-phase for privatization can be moved the function entry by optimizer.
✓ The privatization of parallelization transform pass will move alloca instruction into the outlined function whenever it is necessary.
LLVM Framework Extensions: W-Region

```
#pragma omp target
{ code-block

#pragma omp parallel for
for (k=0; k< N; k++) {
    code-block
    ...... 
}

#pragma omp parallel
code-block
}
```
W-Region Implementation

class WRN { //base class
    BasicBlock *EntryBBlock;
    BasicBlock *ExitBBlock;
    unsigned nestingLevel;
    SmallVector<WRegionNode *,4> Children;
    ...
}

// #pragma omp parallel
class Parallel : public WRN {
    SharedClause *Shared;
    PrivateClause *Private;
    Value NumThreads;
    ...
}

// #pragma omp simd
class Simd : public WRN {
    PrivateClause *Private;
    LinearClause *Linear;
    int Simdlen;
    ...
}
Parallelization and Vectorization Framework

I. Prepare transformation / pre-privatization

II. W-Region graph construction

III. Privatization

IV. Loop partition and scheduling code generation

V. Multi-thread code generation

Scalar IR

Lowering IR

Threaded IR

I. Prepare transformation / pre-privatization

II. Vector function processing

III. W-Region graph construction

IV. VPlan construction

V. VPlan analysis & optimization

VI. VPlan cost modeling

VII. Vector code generation

Operate on VPlan. Input Scalar IR is intact.

Widened Vector IR

Scalar IR
Prepare Transformation Phase

extern float w;

float foo(float *a, float *x, int m)
{
    int k; float y;
    #pragma omp parallel private(k, y, w)
    for (k=3; k< 1000; k++) {
        w = 1.8;
        #pragma omp master
        {
            *x = a[k] + (float)m + w;
        }
        y = *x + k*2.888f; a[k] = k * 1.8 + y;
    }
    printf("a[] = %f\n", a[5]);
    return a[5];
}
Lowering and Outlining Transformation Pass

define float @foo(float* %a, float* %x, i32 %m)
entry:
  %tid.addr = alloca i32, align 4
  %tid.val = call i32 @_kmpc_global_thread_num()
  store i32 %tid.val, i32* %tid.addr, align 4
  ... ...
  store float* %a, float** %a.addr, align 0
  store float* %x, float** %x.addr, align 0
  store i32 %m, i32* %m.addr, align 4
  br label %codeRepl, !dbg !123

codeRepl:
  %fork.test = tail call i32 @_kmpc_ok_to_fork()
  %0 = icmp eq i32 %fork.test, 1
  br i1 %0, label if.then.fork.3,
  label if.else.call.3
if.then.fork.3:
  call void @_kmpc_fork_call(
    {i32, i32, i32, i32, i32, i32, i32, i32, i32} * @loc.9.18,
    i32 3, void (float**,
    i32*, float**) @foo_DIR.OMP.PARALLEL.1,
    float** %a.addr, i32* %m.addr, float** %x.addr)
  br label %DIR.QUAL.LIST.END.8
if.else.call.3:
  call void @foo_DIR.OMP.PARALLEL.1(i32* %tid.addr,
    i32* %bid.addr, float** %a.addr,
    i32* %m.addr, float** %x.addr)
  br label %DIR.QUAL.LIST.END.8

// Outlined Function for the parallel construct
define internal void @foo_DIR.OMP.PARALLEL.1(
  i32* %tid, i32* %bid, float** %a.addr,
  i32* %m.addr, float** %x.addr) #4 {
  newFuncRoot:
    br label %DIR.OMP.PARALLEL.1
  
  DIR.QUAL.LIST.END.8.exitStub:
    ret void
}

DIR.OMP.PARALLEL.1:
  %k.priv = alloca float, align 4 // privatization output
  %y.priv = alloca float, align 4 // privatization output
  br label %DIR.QUAL.LIST.END.2, !dbg !126

DIR.QUAL.LIST.END.2:
  store i32 3, i32* %k, align 4, !dbg !126
  br label %for.cond, !dbg !126

for.cond:
  %0 = load i32, i32* %k, align 4, !dbg !128
  %conv = sext i32 %0 to i64, !dbg !128
  %cmp = icmp slt i64 %conv, 1000, !dbg !128
  br i1 %cmp, label %for.body, label %for.end
...
for.end:
  br label %DIR.QUAL.LIST.END.8.exitStub
Vectorization Example

```c
void foo(int *a, int m)
{
    int k; int y;
    #pragma omp simd lastprivate(y)
    for (k=3; k< 10001; k++) {
        y = a[k];
        if (y > m)
        {
            y = m / y;
        }
        a[k] = k + y;
    }
    printf("y = %d\n", y);
}
```

... ... ...

for.body:

```c
%indvars.iv = phi i64 [ 3, %entry ],
    [ %indvars.iv.next, %if.end ]
%arrayidx = getelementptr inbounds i32, i32* %a,
    i64 %indvars.iv
%0 = load i32, i32* %arrayidx, align 4
%cmp2 = icmp sgt i32 %0, %m
br i1 %cmp2, label %if.then, label %if.end
```

if.then:

```c
%div = sdiv i32 %m, %0
br label %if.end
```

... ... ...
VPlan-based Transformation Pass

VPBlock<1>:
   OriginalBB: for.body:
      ...
   VPBlockSuccessors <4>
      VPBlock<4>:
         OriginalBB: none
         %maskval = vector_mask_to_int(%cmp2)
         %cmp3 = icmp seq i32 %0, %maskval
   VPBlockSuccessors <5> @%cmp3, <3> @%!cmp3
   VPBlock<5>:
      OriginalBB: none
      %0 = select i1 %cmp2, %0, 0x1
   VPBlockSuccessors <2>
      VPBlock<2>:
         OriginalBB: if.then:
            ...
   VPBlockSuccessors <3>
   ...

for.body:
   %indvars.iv = phi i64 [ 3, %entry ],
                  [ %indvars.iv.next, %if.end ]
   %arrayidx = getelementptr inbounds i32, i32* %a,
             i64 %indvars.iv
   %arrayidx1 = bitcast i32* %arrayidx to <4 x i32>*
   %0 = load <4 x i32>, <4 x i32>* %arrayidx1, align 4
   %m1 = ... ; // broadcast %m
   %cmp2 = icmp sgt <4 x i32> %0, %m1
   br label %VPBLOCK4
VPBLOCK4:
   %maskval = bitcast <4 x i1> %cmp2 to <i4>
   %maskval1 = zext <i4> %maskval to <i32>
   %cmp3 = icmp seq i32 %0, %maskval1
   br i1 %cmp3, label %if.end, label %VPBLOCK5
VPBLOCK5:
   %1 = select i1 %cmp2, <4 x i32> %0, <4 x i32> 0x1
   br label %if.then
if.then:
   %div = sdiv <4 x i32> %m1, %1
   br label %if.end
   ...
   ...
Goal: Match ICC SIMD Vectorization

```
#pragma omp simd reduction(+:...)
for(p=0; p<N; p++) {
    // Blue work
    if(...) {
        // Green work
    } else {
        // Red work
    }
    while(...) {
        // Gold work
        // Purple work
    }
    y = foo (x);
    Pink work
}
```

Two fundamental problems:
- ✓ Data divergence
- ✓ Control divergence

Vector code generation has become a more difficult problem increasing need for user guided explicit vectorization that maps concurrent execution to simd hardware.
Summary

- Added a small set of extensions to the LLVM IR that are general enough to represent directives or pragmas.
- Minimized the impact on the existing LLVM infrastructure and scalar and loop optimizations.
- Built (still ongoing) a unified parallelization, vectorization and offloading framework to support for directives (or pragmas) based parallel, vector and offloading language extensions for modern CPUs, GPUs, coprocessors, DSP, and FPGA to explore target HW potential.
- Can produce optimal threaded and/or simdized code by leveraging existing and future scalar and loop optimizations with better interaction among optimization passes.
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